

Vacuum Fluxless Reflow Technology for Fine Pitch

First Level Interconnect Bumping Applications

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Abstract - Heterogeneous integration has become an important performance enabler as high-performance computing (HPC) demands continue to rise. The focus to enable heterogeneous integration scaling is to push interconnect density limit with increased bandwidth and improved power efficiency. Many different advanced packaging architectures have been deployed to increase I/O wire / area density for higher data bandwidth requirements, and to enable more effective die disaggregation. Embedded Multi-die Interconnect Bridge (EMIB) technology is an advanced, cost-effective approach to in-package high density interconnect of heterogeneous chips, providing high density I/O, and controlled electrical interconnect paths between multiple dice in a package.

In emerging architectures, it is required to scale down the EMIB die bump pitch in order to further increase the die-to-die (D2D) communication bandwidth. As a result, bump pitch scaling poses significant challenges in the plated solder bump reflow process, e.g., bump height / coplanarity control, solder wicking control, and bump void control. It's crucial to ensure a high-quality solder bump reflow process to meet the final product reliability requirements. In this paper, a combined formic acid based fluxless and vacuum assisted reflow process is developed for fine pitch plated solder bumping application. A high-volume production (HVM) ready tool has been developed for this process.

Keywords - heterogeneous integration, solder bumping process, fluxless reflow

I. INTRODUCTION

With rising demands for high performance computing (HPC), Heterogeneous integration has become an important performance enabler. The focus to enable heterogeneous integration scaling is to push interconnect density limit with increased bandwidth

and improved power efficiency [1]. Many different advanced packaging architectures have been deployed to increase I/O wire / area density for higher data bandwidth requirements, and to enable more effective die disaggregation. Embedded Multi-die Interconnect Bridge (EMIB) technology is an advanced, cost-effective approach to in-package high density interconnect of heterogeneous chips, providing high density I/O, and controlled electrical interconnect paths between multiple dice in a package.

As the package performance demand goes higher and the yield in the advanced node transistors becomes more challenging, the heterogeneous integration with high bandwidth is crucial in packaging technology [2-6]. With the trend of requiring more functions and performance, bump pitch scaling poses significant challenges in the plated solder bump reflow process, e.g., solder wicking control, bump height / coplanarity control, and bump void control. It's crucial to ensure a high-quality solder bump reflow process to meet the final product reliability requirements.

Formic acid reflow has been developed in industry as a fluxless reflow technology. During the process, formic acid vapor in a nitrogen atmosphere is introduced into the oven as an oxide removal agent. The formic acid vapor reduces tin oxides on the surfaces of the bumps to its elemental state. Thus, the formic acid vapor takes the place of conventional fluxes (pastes in some cases) to assist solder reflow. In addition to acting as a carrier gas for formic acid vapor, the nitrogen atmosphere significantly reduces the presence of atmospheric oxygen within the oven that could lead to reoxidation of metal surfaces prior to reflow.

During the reduction of metal oxides by formic acid, carbon monoxide, carbon dioxide, hydrogen gas, and water are generated as by-products. To remove the toxic and environmental hazardous byproducts, all gases leaving the oven are first passed into burn boxes located at the entrance and exit tunnels of the oven, as well as at the exhaust of the vacuum pump. These burn boxes contain a heated metal catalyst that converts most of the residual formic acid and byproducts into carbon dioxide and water vapor. Catalyst conversion efficiency is a function of formic acid load, catalyst temperature, catalyst age, and measurement technique and is subject to variation with each application. These gases are then passed to the facility exhaust system.

To explore the benefit of this proposed technology, in this paper, modelling and experimental validation have been conducted to analyze solder bump dimension cliff to prevent wicking. Results showed that with different oxide removal agents, the agent activity had a significant impact on solder dimensional cliff. Gas formic acid has higher surface tension compared to regular reflow fluxes, providing the benefit of higher tolerance for solder wicking. Experimental results confirmed that formic acid reflow has benefit in improving bump coplanarity by reducing solder wicking.

One of the primary concerns in solder bumping process is solder void control. Literatures have reported vacuum benefits in solder void reduction [7-9]. In this paper, by combining vacuum during formic acid reflow process, solder void is significantly reduced.

In this work, to mitigate above risks, a combined formic acid based fluxless and vacuum assisted reflow process is developed for fine pitch plated solder bumping application. An HVM ready tool has been developed for this process. We will present in detail the equipment / process technology overview, equipment features, thermal profiles, and characterization results.

II. THEORETICAL ANALYSIS

As described above, during solder bumping process, one of the concerns is solder wicking, which is expected in decreasing bump coplanarity and eventually increasing risk at assembly processes. Many factors are considered to control the wicking risk, such as bump metal stack material, bump geometry and

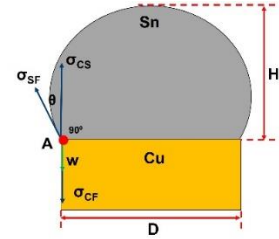


Fig. 1 Force analysis at point A; Point A: contacting point of Cu and Sn; σ_{CS} : surface tension between Cu and Sn; σ_{CF} : surface tension between Cu and flux; σ_{SF} : surface tension between Sn and flux; W: Sn weight; θ : contact angle of Sn wetting on Cu; H: solder bump height; D: bump diameter

dimension, as well as flux agent wetting force. In this study, our focus is mainly on oxide removal agent wetting force's impact on bump dimension cliff.

To maintain adequate solder volume in design, solder bump height (H) needs to go relatively higher when bump diameter (D) is targeting smaller for fine bump pitch, thus driving H/D value increasing. Fig. 1 is an illustration of the force balance at solder and metal pillar interface. In this work, we use Sn as solder material and Cu as pillar metal. At point A, surface tensions at different interfaces (σ_{CS} , σ_{CF} , σ_{SF}) results in the driving forces of Sn wicking. With higher H/D value, it's going to result in higher θ at point A. The max Sn volume that could maintain Sn on top of Cu is determined by solder spread contact angle. Contact angle measurement condition is described in detail in the next session and results are presented in the discussion session.

Another driving force is bulk Sn weight (W) applied at point A, which depends on the solder volume and pad diameter. In this study, solder volume is assumed to be at maximum without any wicking and omitted in the analysis.

III. EXPERIMENTAL CONDITION

A. Vacuum formic acid reflow oven configuration

As described in introduction, an inline convection reflow oven with combined formic acid and vacuum capability has been developed. Tool was configured to deliver maximum process flexibility. The formic acid injection ports in the convection heating zones are adjustable, enabling the formic acid distribution as well as concentration to be fine-tuned to meet different process requirements. The vacuum chamber in this system has two stations, a heating station with IR panel, and a cooling station with water-cooling chill plate. This configuration allows the entire reflow process,

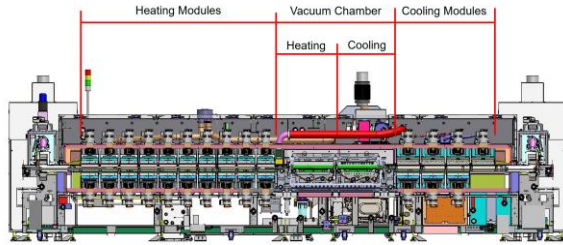


Fig. 2 Oven configuration diagram.

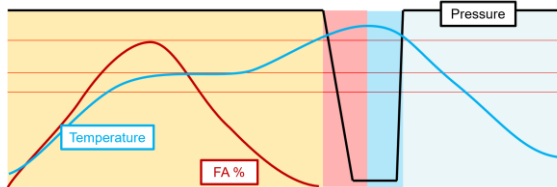


Fig. 3 Typical vacuum formic acid reflow profile and its vacuum formic status.

with all phase change from solid-liquid-solid to be performed under vacuum, which would induce any entrapped void in the molten solder to expand, and expulsion from the solder bump by buoyancy forces. The pump down rate, set point pressure and vacuum dwell time are all programmable for achieving the optimum void reduction results. Oven configuration diagram is shown in Fig. 2.

In a typical process, the board would heat up and soak in formic acid environment to remove oxidation. It would reach and maintain about liquidous as it enters the vacuum state. It would dwell under vacuum to allow for the void to escape, and solidify under vacuum, forming void-free bumps. Fig. 3 is a typical vacuum formic acid reflow profile.

B. Solder spread contact angle measurement

Solder ball contact angle measurement was conducted under following procedures (Fig. 4): 1) Supply flux and set solder ball onto Cu panel; 2) Reflow the coupon under nitrogen environment with a ramping rate of 1C/s from 25 °C to 260 °C; 3) Deflux cleaning for 10 mins; 4) Coupon drying at 150 °C; 5) Solder ball spreading measurement with a standard Video Contact Angle System.

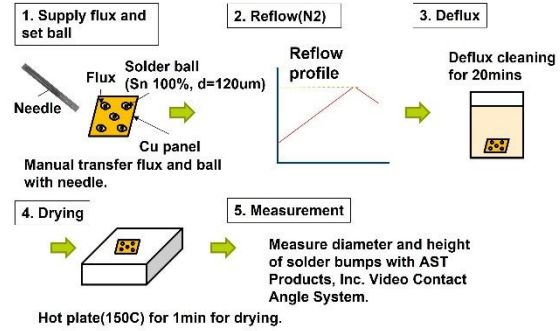


Fig. 4 Solder ball spreading contact angle measurement procedure.

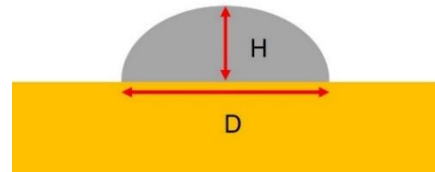


Fig. 5 Side view schematic of solder spread on Cu; D: solder bump spread diameter post reflow; H: solder ball height post reflow.

IV. RESULTS AND DISCUSSION

A. Oxide removal agent wetting analysis

As shown in Fig. 5, solder ball spread diameter (D) and height (H) was measured from top-down view and side view of reflowed solder ball. Thus, the contact angle could be calculated as:

$$\theta = \sin^{-1}\left(\frac{4Dh}{D^2+4H^2}\right) \quad (1)$$

As described above, when Sn volume reaches to the maximum value of maintaining on Cu pillar top without any wicking, the critical angle θ is the solder spread contact angle. Thus, the hemisphere Sn bump height (H) to bump diameter (D) ratio can be calculated as:

$$\frac{H}{D} = \frac{1+\sin\theta}{2\cos\theta} \quad (2)$$

In this study, solder spread contact angle measurement was carried out on three types of oxide removal agent: A, B and formic acid. Flux A has high metal oxide removal rate, flux B has low metal oxide removal rate. Fig. 6 a) shows the contact angle comparison between flux A, B and formic acid. Fig. 6 b) shows the calculated critical H/D cliff from contact angle.

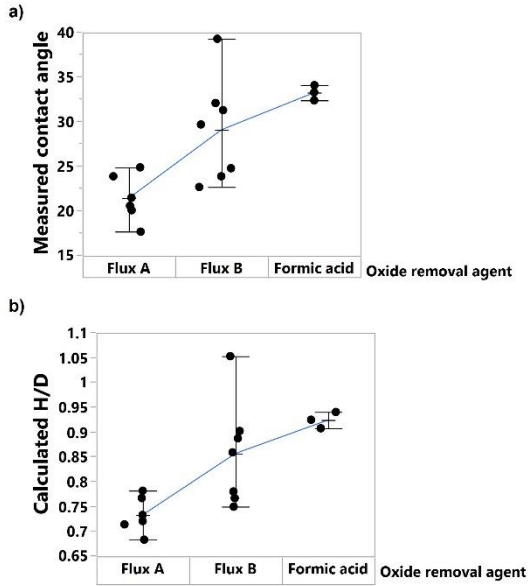


Fig. 6 a) Measured contact angle comparison between flux A, B and formic acid; b) calculated critical H/D cliff from measurement contact angle.

In this test, bump wicking prevention benefit from formic acid is clearly demonstrated. We believe this is mainly due to oxide removal efficiency difference and lower downward driving force (σ_{CF} in Fig. 1). With formic acid reflow process, it can enable higher H/D cliff to provide higher marginality to solder height and solder volume in design. This benefit is becoming more and more important when going with finer bump pitch.

B. Bump coplanarity analysis

From above contact angle measurement and analysis, it is clear that formic acid reflow provides benefits in solder wicking control, which contributes significantly to bump coplanarity at the first level interconnect (FLI). Solder wicking induced bump coplanarity issue can be reflected by low bump defect rate.

In this analysis, we used a test vehicle with H/D ratio of 0.98 to validate the expected benefit. Flux A was used as the control leg. Fig. 7 showed a normalized bump defect rate comparison between two oxide removal agents. Formic acid reflow process can significantly reduce low bump defects. This validates the conclusion that formic acid reflow is bringing in margin improvement in solder height and solder volume control.

C. Bump void analysis

As described in Introduction, another key feature from this work is vacuum capability. By applying vacuum during reflow, it is beneficial to reduce solder voids

while solder is at its liquid phase. This is also validated based on a hammer condition test vehicle sample and measured with 3-D x-ray metrology. Our sample size shown in this paper is about 5800 solder bumps.

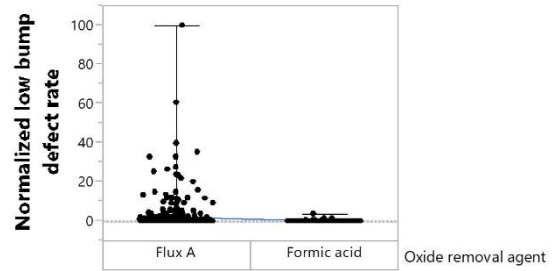


Fig. 7 Normalized low bump defect rate comparison between flux A reflowed sample and formic acid reflowed sample.

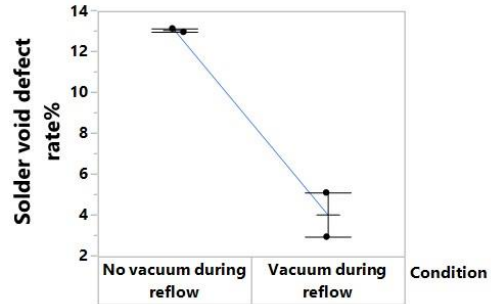


Fig. 8 Normalized 3-D x-ray examination on solder void defect rates.

As shown in Fig. 8, with vacuum capability, solder void defect rate can be reduced significantly. This is consistent with other reported work.

V. CONCLUSION

In this paper, a combined formic acid based fluxless and vacuum assisted reflow process is developed for fine pitch plated solder bumping application. An HVM ready tool has been developed for this process. From theoretical analysis and experimental data, the system shows clear technical advantage of improving solder bump coplanarity, which provides better solder volume and height allowance for fine bump pitch applications. Furthermore, vacuum capability in the system has been demonstrated to provide improvement in solder void reduction.

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VII. REFERENCES

- [1] G. Duan, Y. Kanaoka, R. McRee, B. Nie and R. Manepalli, "Die Embedding Challenges for EMIB Advanced Packaging Technology," 2021 IEEE 71st ECTC 2021, pp. 1-7, doi: 10.1109/ECTC32696.2021.00012.
- [2] B. Sabi, "Advanced packaging in the new world of data", ECTC 2017.
- [3] B. Sabi, Advanced packaging workshop, International Semiconductor Executive Summits 2019.
- [4] H. Azimi, Advanced packaging webinar, International Semiconductor Executive Summits 2020.
- [5] R. Mahajan, "Scaling for heterogeneous integration", Georgia Tech Packaging Research Center Industry-Academic Consortium 2020.
- [6] R. Manepalli, "Advanced packaging technologies for heterogeneous integration: challenges and opportunities", 31st Annual Electronic Packaging Symposium and Semicon West 2019.
- [7] W. Lin, "The Void-free Reflow Soldering of BGA with Vacuum", 2007 8th International Conference on Electronic Packaging Technology.
- [8] T. Ewald, N. Holle, K. Wolter, "Void Formation During Reflow Soldering", 2012 IEEE 62nd Electronic Components and Technology Conference.
- [9] P. Wild, T. Grözinger, D. Lorenz and A. Zimmermann, "Void Formation and Their Effect on Reliability of Lead-Free Solder Joints on MID and PCB Substrates," 2017 IEEE Transactions on Reliability.